What is claimed is:

1. A noise suppression circuit suppressing normal mode noise transmitted on first and second conductive lines and generating a potential difference between the first and the second conductive lines, comprising:

first and second inductors inserted in series in the first conductive line and magnetically coupled to each other; and

a series circuit configured to have a third inductor and a first capacitor connected in series, one end of the series circuit being connected to a junction of the first and second inductors, and other end being connected to the second conductive line,

wherein a coupling coefficient k between the first and second inductors is smaller than 1, and the inductance of the third inductor is set to a value so that a desired noise attenuation characteristic is realized on condition that the coupling coefficient k is smaller than 1.

2. The noise suppression circuit according to claim 1, wherein the inductance L3 of the third inductor satisfies the condition of

$$L3 = k(L1 \times L2)^{1/2} \quad \ldots\ldots (1)$$

where L1 represents inductance of the first inductor, and

L2 represents inductance of the second inductor.

3. The noise suppression circuit according to claim 1, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3>k(L1 \times L2)^{1/2}$ and

$L3 \leq (L1+M) \times (L2+M)/(L1+L2+2M)+M$ ..... (2)

where $M=k(L1 \times L2)^{1/2}$,

L1 represents inductance of the first inductor, and

L2 represents inductance of the second inductor.

4. The noise suppression circuit according to claim 1, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3<k(L1 \times L2)^{1/2}$ and

$L3 \geq 0.9 \times k \times (L1 \times L2)^{1/2}$ ..... (3)

where L1 represents inductance of the first inductor, and

L2 represents inductance of the second inductor.

5. A noise suppression circuit suppressing normal mode noise transmitted on first and second conductive lines and generating a potential difference between the first and the second conductive lines, comprising:

first and second inductors inserted in series in the first conductive line and magnetically coupled to each other;

a series circuit configured to have a third inductor and a first capacitor connected in series; and

fourth and fifth inductors inserted in series in the second conductive line and magnetically coupled to each other,

wherein one end of the series circuit is connected to a junction of the first and second inductors, and the other end is connected to a junction of the fourth and fifth inductors,

each of a coupling coefficient k1 between the first and second inductors and a coupling coefficient k2 between the fourth and fifth inductors is smaller than 1, and the inductance of the third inductor is set to a value so that a desired noise attenuation characteristic is realized on condition that each of the coupling coefficients k1 and k2 is smaller than 1.

6. The noise suppression circuit according to claim 5, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3 = M1+M2$,

$M1=k1 \times (L1 \times L2)^{1/2}$ .....(4-1), and

$M2=k2 \times (L4 \times L5)^{1/2}$ .....(4-2)

where L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.

7. The noise suppression circuit according to claim 5, wherein

the inductance L3 of the third inductor satisfies the conditions of

$L3>M1+M2$ and

$L3 \leq (L1+L4+M1+M2) \times (L2+L5+M1+M2)/\{L1+L2+L4+L5+2 \times (M1+M2)\}+M1+M2$ ..... (5)

where $M1=k1 \times (L1 \times L2)^{1/2}$, $M2=k2 \times (L4 \times L5)^{1/2}$,

L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.

8. The noise suppression circuit according to claim 5, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3<M1+M2$ and

$L3 \geq 0.9 \times (M1+M2)$ ..... (6)

where $M1=k1 \times (L1 \times L2)^{1/2}$, $M2=k2 \times (L4 \times L5)^{1/2}$,

L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.

9. A noise suppression circuit suppressing normal mode noise transmitted on first and second conductive lines and generating a potential difference between the first and the second conductive

lines, comprising:

first and second inductors inserted in series in the first conductive line and magnetically coupled to each other;

a series circuit configured to have a third inductor and a first capacitor connected in series; and

fourth and fifth inductors inserted in series in the second conductive line and magnetically coupled to each other and magnetically coupled to the first and second inductors,

wherein one end of the series circuit is connected to a junction of the first and second inductors, the other end is connected to a junction of the fourth and fifth inductors,

each of a coupling coefficient k1 between the first and second inductors, a coupling coefficient k2 between the fourth and fifth inductors, a coupling coefficient k3 between the first and fourth inductors, a coupling coefficient k4 between the second and fifth inductors, a coupling coefficient k5 between the first and fifth inductors, and a coupling coefficient k6 between the second and fourth inductors is smaller than 1, and the inductance of the third inductor is set to a value so that a desired noise attenuation characteristic is realized on condition that each of the coupling coefficients k1, k2, k3, k4, k5, and k6 is smaller than 1.

10. The noise suppression circuit according to claim 9, wherein

the inductance L3 of the third inductor satisfies the conditions of

$L3 = M1+M2+M5+M6$,

$M1=k1 \times (L1 \times L2)^{1/2}$ .....(7-1),

$M2=k2 \times (L4 \times L5)^{1/2}$ .....(7-2),

$M5=k5 \times (L1 \times L5)^{1/2}$ .....(7-3), and

$M6=k6 \times (L2 \times L4)^{1/2}$ .....(7-4)

where L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.

11. The noise suppression circuit according to claim 9, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3>M1+M2+M5+M6$ and

$L3 \leq (L1+L4+M1+M2+2 \times M3+M5+M6) \times (L2+L5+M1+M2+2 \times M4+M5+M6)/\{L1+L2+L4+L5+2 \times (M1+M2+M3+M4+M5+M6)\}+M1+M2+M5+M6$ ..... (8)

where $M1=k1 \times (L1 \times L2)^{1/2}$, $M2=k2 \times (L4 \times L5)^{1/2}$, $M5=k5 \times (L1 \times L5)^{1/2}$, $M6=k6 \times (L2 \times L4)^{1/2}$,

L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.

12. The noise suppression circuit according to claim 9, wherein the inductance L3 of the third inductor satisfies the conditions of

$L3<M1+M2+M5+M6$ and

$L3 \geq 0.9 \times (M1+M2+M5+M6)$ ..... (9)

where $M1=k1 \times (L1 \times L2)^{1/2}$, $M2=k2 \times (L4 \times L5)^{1/2}$, $M5=k5 \times (L1 \times L5)^{1/2}$, $M6=k6 \times (L2 \times L4)^{1/2}$,

L1 represents inductance of the first inductor,

L2 represents inductance of the second inductor,

L4 represents inductance of the fourth inductor, and

L5 represents inductance of the fifth inductor.